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Purpose

- Amplify (boost) weak signal
- Remove noise or other unwanted signal components
  - filtering
  - common mode rejection
- Preprocess signal for later operations
  - Attenuate high frequencies: anti-aliasing before
- A/D conversion
Basic electronics

Operational Amplifiers (Op-Amps)

\[ | V_+ |, \ | V_- | \text{ usually between 0 and 25 volts} \]
Op-Amp Features

1. Very high gain | \( e_o / e_i \) | = \( A = 10^6 \) to \( 10^8 \)

2. Large bandwidth (MHz or more)

3. High input impedance \( R_i \approx 100 \, k\Omega \) to \( 100 \, M\Omega \)
   \( \Rightarrow \) small input load currents

4. Low output impedance \( R_o \approx 10^1 \) to \( 10^2 \, \Omega \)

5. Differential inputs \( e_i = e_a - e_b \)

6. High Common Mode Rejection Ratio (CMRR) \( \approx 50 \) to \( 100 \) dB. \( \text{dB} = 20 \log_{10} \)

   CMRR: same common mode signal \( e_{CM} \) into \( e_a \) & \( e_b \) \( \Rightarrow \) tiny \( e_o \)
   If channel a & b input impedances same, minimizes effect of signals induced on both channels (e.g. 60 Hz from building supply).

   Common Mode Gain: \( \text{CMG} = A / \text{CMRR} \) (e.g., \( = 10^6 / 10^5 \approx 10 \)).

7. Temperature dependent parameters: design to minimize effects.

8. Voltage Supply Rejection Ratio (VSRR) gauges effect of power supply drift & variations \( V_+ \) and \( V_- \) as equivalent input \( e_i \).

9. Input Offset voltage \( V_{\text{offset}} \): Manufacturing imperfections & temperature variations \( \Rightarrow e_o \neq 0 \) when \( e_i = 0 \) (violating desired \( e_o = -A \cdot e_i \)). To correct, adjust \( V_{\text{offset}} \):
\( V_{\text{offset}} \) allows low cost Op-Amp. Imperfections corrected (cheaply) at installation, not (expensively) during chip manufacture.


Output \( V_- \leq e_o \leq V_+ \Rightarrow \frac{V_-}{A} \leq -e_i \leq \frac{V_+}{A} \).

11. Input bias currents \( I_+ \) and \( I_- \) (10 nA to \( \mu \)A) flow through + (b) and - (a) input terminals to bias input transistors (FET gate or BJT base). Voltage drop developed across input elements must be balanced (same at both terminals) so that \( e_o = 0 \). \( \Rightarrow \) Balanced input resistances to + and - .

12. Input offset currents \( I_+ \) and \( I_- \) \( \Rightarrow \) residual \( e_o \neq 0 \) unless minimized with potentiometer on one input to fine tune. Can also adjust \( V_{\text{offset}} \). Puts upper limit on values of input resistors (minimize voltage drops due to \( I_+ \) and \( I_- \)).
13. Class B operation often used in output stage: complementary npn & pnp in push/pull (Nearly identical amplifier circuits--stage 1 & stage 2--arranged in parallel. Stage 1 amplifies only positive voltages, and switches off for negative. Stage 2 amplifies only negative, and switches off for positive.) Crossover distortions possible (small signals) in dead space as transistors in stages switch on/off.
Other Op-Amp Specifications & Issues

A. **Slew rate** $SR = \lim_{t \to \infty} \frac{\text{de}_o}{\text{dt}}$ important to avoid large signal distortions.

$$e_i = E \sin \omega t; \quad SR = E \omega \cos \omega t \bigg|_{\text{max}} = E \omega$$

*Require* $SR \geq 2\pi f E$ for amp to follow largest voltage swing.

B. **Compensation:** Lead/lag network to control phase margin when negative feedback. For stable amplifier design gain ($-\frac{R_2}{R_1}$ for inverting amplifier, $1 + \frac{R_2}{R_1}$ for noninverting amplifier), require closed loop response curve to meet open loop curve where slope of closed loop curve is $-20 \text{ dB/dec}$.

- $-20 \text{ dB/dec} \Rightarrow 1^{\text{st}} \text{ order term} \Rightarrow -90^\circ \text{ phase} \Rightarrow \text{limited signal growth (phase margin} = 180^\circ - 90^\circ = 90^\circ \Rightarrow \text{stable closed loop system})$

Internally compensated: manufacturer provides network for $-20 \text{ dB/decade}$; limits bandwidth but unconditionally stable.

Externally compensated: Install capacitance ($\approx \mu\text{F}$) across indicated frequency compensation terminals to control bandwidth and closed loop gain ($-40 \text{ dB} \Rightarrow -20\text{dB}$).

Manufacturer specifies needed capacitance. Conditionally stable (for given closed loop gain).
Unstable Feedback Oscillation: Sinusoid grows

First cycle: No feedback, but GH inverts. First cycle: Negative feedback & GH inversion (-360° phase) add constructively with input.

After second pass, feedback promotes signal growth. Further passes ⇒ unstable!
C. Power Supply Filter Capacitors (10⁻¹ to 1 µF) to minimize power supply fluctuations
Amplifier Configurations

Inverting amplifier

\[ \begin{align*}
&\text{a. DC analysis} \\
&\text{DC biases: Very large } R_i \Rightarrow e_{ab}^{DC} \approx 0 \Rightarrow e_a^{DC} \approx e_b^{DC} \\
&\text{Small bias current } i_3^{DC} \approx 0 \Rightarrow e_b^{DC} = - i_3^{DC} R_3 \approx 0 \\
&\Rightarrow e_a^{DC} = 0 : \text{node a at virtual ground!} \\
&\text{Negative feedback (via } R_2) \text{ enhances.}
\end{align*} \]
b. \[ R_3 = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \] to balance input bias current voltage drop:

If \( R_3 = 0 \), \( e_a^{DC} \approx e_b^{DC} = 0 \Rightarrow i_1^{DC} = 0 \) & \( i_2^{DC} = \frac{e_o^{DC} - e_a^{DC}}{R_2} \)

\[ e_o^{DC} = i_2^{DC} R_2 \neq 0 \]

Required: zero input \( e_s = 0 \) \( \Rightarrow e_o = e_o^{DC} + e_o^{AC} = 0 \).

Achieved via \( R_3 = R_1 \parallel R_2 \)
(balanced bias currents \( i_3^{DC} = i_1^{DC} + i_2^{DC} \)).

c. AC signal analysis

Currents into – inverting terminal negligible (very large \( R_i \)) \( \Rightarrow i_1 \approx -i_2 \)

\[ \Rightarrow \frac{e_s - e_a}{R_1} = -\frac{e_o - e_a}{R_2}, \]

with \( e_o = -A \ e_i = -A (e_a - e_b) = -A \ e_a \)

\[ \frac{e_o}{e_s} = -\frac{A}{1 + R_1/R_2 (1 + A)} \approx -R_2/R_1 \text{ at low freq. } A \gg 1 \]

breaks down at high freq. \( A = A(f) \) & \( R_i = R_i(f) \)

d. Input resistance \( R_{in} = \frac{e_s}{i_1} = \frac{e_s R_1}{e_s - e_a} \approx R_1 \text{ at low frequency} \)

e. Output resistance \( R_{out} \approx \frac{R_0 (1 + R_1/R_2)}{A} \text{ small} \)

\((10^{-1} \text{ to } 10^0)\)
Multiple Inputs: Sum Over Inverting Point

\[ e_0 \approx -R_2 \left\{ \frac{e_1}{R_{11}} + \frac{e_2}{R_{12}} + \frac{e_3}{R_{13}} \right\} \]

\[ R_3 = (R_{11} \ | \ R_{12} \ | \ R_{13}) \ | \ R_2 \]
Three Resistor Equivalent Feedback Network

Equivalent feedback resistor \( R_2 = R_{2a} + R_{2b} + R_{2a} \frac{R_{2b}}{R_{2c}} \)

Small \( R_{2c} \Rightarrow \) large equivalent \( R_2 \) without big (noisy) resistors

For higher gain Op-amp designs
Non-inverting Amplifier

\[ R_3 = R_1 \parallel R_2 \]

a. Input on non-inverting + terminal, feedback to inverting - terminal for stability

b. \[ \frac{e_o}{e_s} = \frac{A}{1 + A R_1 / (R_1 + R_2)} \]

\[ \approx 1 + \frac{R_2}{R_1} \text{ @ low freq, } A \gg 1 \]

c. Input resistance \( R_{\text{in}} \approx \frac{R_i A}{1 + R_2/R_1} \gg R_i \) extremely large

d. Output resistance \( R_{\text{out}} \) same as inverting amp.
Differential Amplifier

\[ R_2 \]

\[ e_{s1} \]

\[ R_1 \]

\[ e_{s2} \]

\[ e_o \]

\[ R_3 \]

\[ R_4 \]

a. Common mode rejected (e.g., drift) via high CMRR

\[ R_3 = R_1 \]

b. \[ e_o \approx \frac{R_4}{R_3 + R_4} \left(1 + \frac{R_2}{R_1}\right) e_{s2} - \frac{R_2}{R_1} e_{s1} = \frac{R_2}{R_1} \left(e_{s2} - e_{s1}\right) \]

\[ R_4 = R_2 \]

c. \[ R_{in}^- = R_1 \text{ (small)} \quad R_{in}^+ \approx R_3 + R_4 \text{ (small)} \]
Instrumentation Amplifier

Combine advantages:
High input impedance / non-inverting terminals
Differential stage (CMRR)
Design Guidelines

A. Op-Amp selection
   Gain & bandwidth within scope of amp design
   Peak to Peak output voltage swing within range of supply rails ($V_+, V_-$)
   Slew rate $SR \geq \frac{dv}{dt} \big|_{max}$
   Acceptable noise figure (NF) over operating range

B. Stability
   Frequency compensation (internal or external) for
   -20 dB/dec
   External: resistors and capacitors specified by manufacturer
   -20 dB/dec. at desired gain ⇒ stable amplifier

C. Power supply
   Supply rails $V_+, V_-$ sufficient for swings
   minimize power supply fluctuations with
   filter capacitors
   avoid draining: power peaks sufficient
   $V_+, V_-$ not too high: excessive shot noise
D. Resistor selection
\[ R_{\text{in}} = R_1 \quad R_{\text{min}} < R_1 < R_{\text{max}} \]
- \( R_{\text{min}} \) lower bound from signal source (i, v)
- impedance: want high \( R_{\text{max}} \) limited by
  offset current \( \Rightarrow \) DC drop at output &
  thermal noise

\[ V_{\text{oc}} = [R_1 \parallel R_2] i_{\text{oc}} \max < 10\% \text{ max allowed distort; } \]
- \( i_{\text{oc}} \): offset current
- \( R_2 / R_1 \) gain for inverting amp, \( 1 + R_2 / R_1 \)
- for non-inverting amp
- \( R_3 = R_1 \parallel R_2 \)
- Networks (manufacturer)
  - voltage offset
  - compensation

E. Offset (defined by \( e_i = 0 \Rightarrow e_o \neq 0 \))

\[ V_{\text{oc}} \ll V_{\text{offset}} \]
- \( V_{\text{offset}} \) reduced via voltage offset
- temperature dependence within operating range
  - zero at \( T_{\text{operating}} \)
  - \( \delta V_{\text{out}} \) for \( \delta T < \) allowable distortion

F. Distortion components (total < allowable)
- common mode / bias current (CMRR)
- \( V_{\text{oc}} \)
- \( \delta V_{\text{out}} \)
- power supply fluctuations (VSRR)
- insufficient bandwidth, slew rate, supply rails
Passive Element Filters

T network

π network

Goal: overall impedance = Z_{load}

Capacitor: C, Inductor: L, low cutoff frequency: f_l, high cutoff frequency: f_h

Designs:

Low pass: Z_1 = L, Z_2 = C, f_l = 0, f_h = \frac{1}{\pi \sqrt{LC}}

High pass: Z_1 = C, Z_2 = L, f_l = \frac{1}{4\pi \sqrt{LC}}, f_h = \infty

Bandpass: Z_1 = L_1 \text{ series } C_1, Z_2 = L_2 \text{ } || \text{ } C_2,
\quad f_l, f_h \text{ depend on } Z_{load}

Bandreject: Z_1 = L_1 \text{ } || \text{ } C_1, Z_2 = L_2 \text{ series } C_2,
\quad f_l, f_h \text{ depend on } Z_{load}
Basic Op-Amp Active Filters

1st order active filter

\[
\begin{align*}
\text{Inverting amp with feedback C & } R_2: \\
H(s) &= \frac{e_o(s)}{e_s(s)} = -\frac{R_2 \ || \ 1/sC}{R_1} = -\frac{R_2}{R_2C} \frac{1}{s+1} \\
\text{low frequency gain:} & \quad \frac{R_2}{R_1} \\
\text{3 dB cutoff frequency:} & \quad f_c = \frac{1}{2\pi R_2C}
\end{align*}
\]
Non-inverting amp with coupling capacitors. Low frequency gain: \( K = 1 + \frac{R_b}{R_a} \)

\[
H(s) = \frac{e_o(s)}{e_s(s)} = \frac{K}{s^2 R_1 R_2 C_1 C_2 + s [R_2 C_1 + R_1 C_1 + (1 - K) R_1 C_2] + 1}
\]

cutoff (natural) frequency: \( f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \)
2nd order active filter, High gain type

Inverting amp with feedback $C_2$ \parallel (R_4 + R_2), \text{ input } R_1 + R_2, \text{ coupling capacitor } C_1

$$H(s) = \frac{e_o(s)}{e_s(s)} = -\frac{1/R_1 R_2 C_1 C_2}{s^2 + s [1/R_1 + 1/R_4 + 1/R_2](1/C_1) + 1/R_4 R_2 C_1 C_2}$$

cutoff (natural) frequency: \[ f_c = \frac{1}{2\pi\sqrt{R_4 R_2 C_1 C_2}} \]

Higher order filters usually cascade 1st & 2nd order filters
Analog Integrator

Inverting amp with feedback C & input R
Replace feedback R with impedance 1/sC:

\[ H(s) = \frac{e_o(s)}{e_i(s)} = -\frac{1/sC}{R} = -\frac{1}{sRC} \]

Integrator: \[ e_o(t) = -\frac{1}{RC} \int e_o(t) dt \]
R2R Resistance Ladder

Enables digital (software) control of resistance
Input resistance can be changed in-situ

\[ V_i \frac{2R}{R} \frac{R}{2R} \frac{2R}{2R} \frac{2R}{2R} \frac{2R}{Z} \frac{V_o}{-} \frac{+}{=} \]

operation
switches control currents to terminals:
non-inverting (ground)
inverting terminals (virtual ground)
total ladder current constant
currents half (left to right), each ladder step

resistance into op-amp looking into any node: R
2R \| 2R
currents split in half
Digital to Analog Converters (D/A or DAC)

Converts digital (binary number) to analog voltage

Settling time $t_s$:
- time required for analog input (voltage or current) to settle within $\pm$ LSB/2 following input code change

- typical: nsec to 100 µsec
- circuits downstream add dynamics $\Rightarrow$ increases $t_s$
D/A: Weighted Current Sources

Switch function \( a_k = \begin{cases} 
1, & S_k \text{ closed} \\
0, & S_k \text{ open} 
\end{cases} \)

controlled by bit settings

"Bit" currents \( i_k \) sum, give output:

\[
V_o = -V_s R_2 \sum_{k=0}^{3} \frac{a_k}{R_{1k}}
\]

Problems:

Many bits ⇒ many resistors

Usually \( R_{1k} = 2^k R \) for binary powers

requires accurate resistors: each resistor must be \textbf{precisely} \( 1/2 \) its neighbor
DAC: R2R Ladder Network

R2R Ladder Network DACs in 8, 10, 12, 14, 16, or 18 bits

Output $V_o$ more accurate: only 2 resistor values needed

similar to weighted current source: currents in powers of 2

noninverting terminal at ground, inverting terminal at virtual
ground ⇒ ladder currents constant, independent of switches

Example: 4 bit D/A (Bits 3, 2, 1, 0)

\[
2R i_0 = V_0 = 2R i_t \quad \Rightarrow \quad i_0 = i_t
\]

\[
2R i_1 = V_1 = R(i_0 + i_t) + V_0 \quad \Rightarrow \quad i_1 = 2i_0
\]

\[
2R i_2 = V_2 = R(i_1 + i_0 + i_t) + V_1 \quad \Rightarrow \quad i_2 = 2i_1
\]

\[
i = \sum_{k=0}^{3} a_k i_k;
\]

\[
V_o = \sum_{k=0}^{3} a_k \frac{R_2}{2R} V_k = -R_2 \sum_{k=0}^{3} a_k i_k = -R_2 i
\]
Sample and Hold Circuits

In higher performance A/D converters
Operation (Sample & Hold Input during A/D conversion)
switch (FET) closes & analog voltage charges capacitor
capacitor voltage to Op-Amp constant (held) after switch opens

MOSFET:
Positive gate voltage attracts electrons (charge carriers)
into channel, increasing conductance
FET "switch" characteristics
\[ V_{GS} \text{ low} \rightarrow 10 \, \text{M} \Omega \text{ (open switch)} \]
\[ V_{GS} \text{ high} \rightarrow 200 \, \Omega \text{ (closed switch)} \]
Comparator: Special Op-Amp circuit prone to saturation, but optimized for fast recovery from saturation

\[ V_+ \text{ (high), } V_1 > V_2 \]

\[ V_{\text{out}} = \begin{cases} 
V_- \text{ (low), } V_1 < V_2 
\end{cases} \]

![Comparator Diagram](image)
Analog to Digital Converters (A/D or ADC)

Convert analog voltage to digital (binary)

1) A/D Successive Approximation

Input frozen by sample & hold
Diodes limit $V_d$ swing due to $I = \frac{V_{in}}{R} - I_{test}$

series of n (# bits) bit tests places input in bin (voltage range)
D/A converter generates test currents $I_{test}$ (or voltages), to be compared to input

final D/A number = A/D result
$I_{test}$ reflects current D/A setting

$I = \frac{V_{in}}{R} - I_{test} \Rightarrow V_d \Rightarrow$ high or low logic
Test sequence, 4 bit A/D ⇒ 4 tests

<table>
<thead>
<tr>
<th>test</th>
<th>bit tested</th>
<th>D/A test setting</th>
<th>bit test result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3 (MSB)</td>
<td>0111</td>
<td>a3</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>a3 011</td>
<td>a2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>a3 a2 01</td>
<td>a1</td>
</tr>
<tr>
<td>4</td>
<td>0 (LSB)</td>
<td>a3 a2 a1 0</td>
<td>a0</td>
</tr>
</tbody>
</table>

\[
 a_k = \begin{cases} 
 1, & V_d > 0 \Rightarrow I_{test} < V_{in} / R \\
 0, & V_d < 0 \Rightarrow I_{test} > V_{in} / R 
\end{cases}
\]

Bit test result \( a_k \) causes D/A to output current \( I_{test} \) that CANCELS a component of input current \( V_{in} / R \), thereby fine tuning D/A register. Final result \( a_3 a_2 a_1 a_0 \).

Problem: accurate but moderate speed. Conversion times 1 \( \mu s \) to 100 \( \mu s \).
Capacitor Based Successive Approximation

- Charge all capacitors to $V_{in}$
  - lower plate = input voltage $V_{in}$
  - upper plate = ground
- For ADC, Switch
  - leftmost C (MSB) to $+V_{ref}$
  - other C's to $-V_{ref}$
  - ground switch open
- Comparator determines if
A/D Parallel Flash ADC converters

Speeds exceed 500 MHz: up to 4 GHz for 4 bit converter
Voltage dividing resistors R create $2^n$ voltage levels or “bins”
Comparators ⇒ which "bin" contains input

Big Problem: need $(2^n - 1)$ resistors & comparators for $2^n$ bins
⇒ requires large silicon area on chip
⇒ usually limited to 3 to 6 bits

Other problems:
   parasitic capacitance at each resistor limits bandwidth
   many resistors increase power consumption
Pipelining

- Sample & Hold (S/H)
- Multiple conversion stages
- 1 or 2 bit conversions @ each stage
  - Flash converters do ADC
  - DAC converts bits to voltage
  - Subtract bit voltage from input, create residue
  - Amplify residue
  - Next stage does next bits
  - Order: MSB to LSB
- Pipeline: Samples flow through, 1 stage at a time

Advantages
N to 2N COMPARATORS
High sampling frequency, with > 8 bits

Drawbacks
Complexity
Power consumption
Sigma Delta $\Sigma\Delta$ (Delta Sigma $\Delta\Sigma$) Converters

For low frequency signals
Output: pulses of constant amplitude & duration
Interval between pulses proportional to input voltage.
Higher input voltage ⇒
⇒ Greater slope of integrator output (~ramp) voltage @4
⇒ More frequent comparator triggers & spikes @5
⇒ Shorter intervals between pulses @2 & @3
Count pulses: count ~ input voltage
Hybrid Digital/Analog Systems

Noise perspective: analog & digital systems incompatible
  analog contaminated by digital pulses $\Rightarrow$ AC noise via
  power supply feedback
  stray C's
  ground loops
  digital contamination
  analog $\Rightarrow$ lower frequency filtering
  reduced digital pulses

Prescription: Isolate systems
  1. Separate analog & digital grounds
  2. Connect digital & analog at ONE point ONLY
     (avoid ground loops)
  3. Provide separate analog & digital supply voltages
  4. Electrostatic shielding (Faraday cage) around
     analog circuit. Connect one end only to analog
     ground
  5. At especially sensitive interconnections, consider
     electro-optic coupling
  6. Consider using emitter coupled logic (ECL) in
     digital section for less spurious signal generation
  7. If analog & digital on same IC, separate with wells
     (pn junctions)