Effect of barrier process on electromigration reliability of Cu/porous low-k interconnects

Jung Woo Pyun, Won-Chong Baek, Jay Im, and Paul S. Ho
Microelectronics Research Center, PRC/MER Mail Code R8650, The University of Texas at Austin, Austin, Texas 78712-1000
Larry Smith, Kyle Neuman, and Klaus Pfeifer
SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741

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Electromigration (EM) reliability of Cu/low-k interconnects with a conventional preclean-first process, and an advanced barrier-first process has been investigated. Compared with the preclean-first process, extrinsic early failures were not observed for the barrier-first process. This suggests that process-induced defects, which are the most probable cause for early failures, are significantly reduced for the barrier-first process. Transmission electron microscopy observation demonstrated a more uniform and thicker Ta barrier for the barrier-first process than the preclean-first process. This led to a higher \((jL)_c\) product, and prolonged the EM lifetime accordingly. In addition, a predeposited Ta barrier during the barrier-first process protected the mechanically weak low-k dielectrics from plasma etch damage, and a uniform via profile resulted. In contrast, the via opening at the top was found to be larger than that of at the via bottom for the preclean process. The uniform via profile is another advantage of the barrier-first process from the point of view of process control. © 2006 American Institute of Physics. [DOI: 10.1063/1.2219003]

I. INTRODUCTION

With the implementation of low-k dielectrics in Cu damascene interconnects, the Ta(N) barrier formation process has become important for preventing the Cu diffusion into adjacent dielectrics. Continuous shrinkage of device features necessitates the accompanying reduction of the barrier thicknesses, while maintaining required performance as a diffusion barrier and adhesion promoter. Significant efforts have been expended on developing barrier materials and process technologies to satisfy these requirements.1

In a conventional dual-damascene process scheme, known as the preclean-first process, the barrier layer deposition step follows the argon sputter preclean to remove copper oxide and the dry etch residues. Low-k dielectrics, being mechanically weak, are more prone to plasma damage during the preclean process. In addition, copper oxide or etch residues removed from via bottom possibly redeposit on the via sidewall, causing reliability degradation.2 In contrast, the barrier-first process has been demonstrated to help alleviate these issues.3 The barrier-first process enables one to reduce critical dimension (CD) loss and minimize copper contamination, which was a problem in the preclean process. In addition, the low-k dielectric is protected from the argon plasma damage during an argon etchback by the first-deposited barrier layer. The improvement of via resistance, interlayer dielectric reliability, via stressmigration and electromigration (EM) performance by the barrier-first process compared with the conventional preclean first process was reported by Alers et al.4 However, a systematic study on the barrier-first process effect on electromigration has not been reported.

EM is a serious reliability issue, particularly with line-width scaling down and the implementation of thermomechanically weak low-k dielectrics. Many studies have found that the surface diffusion between Cu and capping layer, such as SiN, is the most dominant mass transport path in the Cu interconnects. This is because the Cu surface, in contact with the cap, contains defects caused by chemical mechanical polishing (CMP), which is a necessary step in the damascene process.4–6 It is for this reason that the most recent studies have mainly focused on reducing the surface diffusion by adding an overcoating layer, such as CoWP, Pd, CoSnP, etc., on top of the Cu layer after the CMP process.7,8 With the surface diffusion contained in this manner, efforts are now focused on a few other areas for controlling electromigration, such as barrier thickness and via processing. Among these areas, the barrier thickness continues to scale down by following the ITRS roadmap, which in turn lowers critical current density and line length \((jL)\), product. The critical length effect leading to the \((jL)_c\) product was first advanced by Blech,9 and many studies followed in the Cu/oxide and Cu/low-k interconnects.10–12 They reported that the \((jL)_c\) product of the Cu/low-k interconnects was lowered due to mechanically weak low-k dielectric compared with an oxide. The other area, via processing, represents a portion of dual-damascene process, the dominant scheme for the fabrication of Cu interconnects. It can inflict plasma damage and process-induced defects at the via bottom and an uneven coverage of barrier layer at the sidewall. These problems manifest in electromigration early failures and stress migration failures.

In our previous studies,13 with decreasing Ta barrier thickness, the critical current density and line length \((jL)_c\) product was found to be lowered. This was attributed to the
reduced confinement effect. Also, a bimodal failure distribution was found, which was attributed to copper outdiffusion through thin Ta barrier. In this work, we investigated the effect of the barrier-first process on EM reliability, and compared the results with those of the conventional preclean-first process. In addition, we studied the Ta barrier thickness effect on EM using the barrier-first scheme. For a determination of both the critical current density and line length \((jL)\), product and early failure statistics, multilinked EM test structures were built and utilized.

II. EXPERIMENTAL DETAILS

Two types of multilinked test structures were designed to determine \((jL)\), products and statistical early failure populations. The critical length (LC) structures were comprised of six repeating multilinked structures with the stressing M2 length varying from 10 \(\mu\)m to 300 \(\mu\)m, while the connecting M1 line length remaining constant at 5 \(\mu\)m in order to prevent EM in the M1 lines. The second multilinked structure was an early failure (EF) structure, which contained a different number of line segments, ranging from one \((N=1)\), ten \((N=10)\), and one hundred \((N=100)\) test structures in series. Two distinct EF test structures were designed. One was an up-current test structure designed to investigate EM damage in a dual-damascene trench and via on M2 level. In this structure, stressed M2 lines were 0.175 \(\mu\)m wide and 150 \(\mu\)m long, while connecting M1 lines remained wide and short. For the down-current test structures, designed for EM on M1 level, we reversed the line dimensions.

Test samples were fabricated at Sematech using a dual-damascene process scheme. The low-k intermetal dielectric layer used in this study was porous methylsilsesquioxane, which is a spin-on organosilicate material with \(k \approx 2.3\). Three types of Ta barriers were integrated at the M2 and via levels. The three splits were comprised of the preclean-first scheme, thin barrier-first scheme, and thick barrier-first scheme. The integration procedure at the M1 level was identical for all three splits. EM experiments were performed in a vacuum chamber with a pure nitrogen environment at 20 Torr, heated at a rate of 5 \(^\circ\)C/min to a target temperature, with a current chamber with a pure nitrogen environment at 20 Torr, heated three splits. EM experiments were performed in a vacuum integration procedure at the M1 level was identical for all thin barrier-first scheme, and thick barrier-first scheme. The three splits were comprised of the preclean-first scheme, and thick barrier-first scheme. The integration procedure at the M1 level was identical for all three splits. EM experiments were performed in a vacuum chamber with a pure nitrogen environment at 20 Torr, heated at a rate of 5 \(^\circ\)C/min to a target temperature, with a current density of 1.0 MA/cm\(^2\). The resistance changes as a function of time were measured and recorded. The time at the first appreciable line resistance increase (usually \(\approx 10\%\)) was taken as the failure time. From the lifetime data, the cumulative failure distribution (CDF) was obtained as a function of time. Then, Monte Carlo simulation was performed to generate new CDF curves which fit the data for the entire time span.\(^{14}\) The parameters deduced from the fit were used to determine the probability of EF and to separate the weak mode distribution from the strong mode. To derive the statistical \((jL)\), products for each split, void distributions as a function of line length of the EM failed samples were determined with the aid of an optical microscope. It is assumed that the EM failure probability of a metal line was proportional to its average drift rate.\(^9\) Therefore, an increasing statistical occurrence of failures was observed in the longer lines due to a smaller back-flow stress and accompanying faster net drift velocity gradient. The analysis of the microstructure, including the Ta barrier morphology and EM induced voids, was performed by a transmission electron microscopy (TEM) and a focused-ion-beam microprobe.

III. RESULTS AND DISCUSSION

The CDF, as a function of time is shown in Fig. 1 for the sample with the preclean-first process [Fig. 1(a)], and thin barrier-first process [Fig. 1(b)]. For reference, the barrier thicknesses of the various processes were obtained from TEM images, and are plotted in Fig 4. For the preclean-first samples, bimodal failure distribution was observed indicating that two different EM failure mechanisms were involved. The probability of EF derived using Monte Carlo simulation,\(^{14}\) was 0.15%. This signifies that about 1.5 interconnects out of 1000 will be failed by extrinsic failure mode. In contrast, the CDF for the barrier-first process demonstrates a monomodal failure distribution for all line segments examined. We project that process-induced defects in the via bottom, which are a primary cause of the EFs, are significantly reduced by the barrier-first process, leading to an improvement of EM reliability. In comparison, the preclean-first process was affected by process-induced defects. For example, Cu contamination—caused by sputter-etch preclean—degrades the Ta barrier adhesion at the via sidewall.\(^3\)

![CDF Plots of EM test results using EF test structures with preclean-first process (a) showing bimodal failure distribution, and (b) barrier-first process showing the monomodal failure distribution, indicating the improvement of EM reliability.](image-url)
however, it can be unfavorable for the leakage current and uneven via profile may not affect EM reliability directly, the top is larger than that of at the via bottom, while a uniform and vertical via is found for barrier-first process. The TEM images, shown in Fig. 2, help explain other differences between the two processes. For the preclean-process, the via opening at the top is smaller than that of at the via bottom, while a uniform and thinner Ta barrier for the preclean-first process, leads to a lower current density and thinner Ta barrier. The TEM images, shown in Fig. 2(b), support our interpretation of the EF EM test results. The images clearly show the different via bottom and sidewall morphologies between the two processes. For example, the degree of via recess into the M1 was more significant in the preclean-first process than in the barrier-first process. Such a recess, attributable to the argon plasma preclean process, creates a notch-shaped point as shown in Fig. 2(a), which can develop stress concentration to cause a stress-induced delamination problem under high-temperature EM test conditions. This can lead to an extrinsic failure, which is not an issue with the barrier-first process as shown in Fig. 2(b). The fuzzy interface of the Ta barrier, shown in Fig. 2(b), was most likely developed due to the argon plasma preclean process, which caused the damage to and roughness of the low-k surface at the via sidewall. The uneven low-k surface, in turn, affected the Ta barrier deposition process which followed. A thin outdiffused metal layer, considered to be the Ta barrier, was found in the high-resolution TEM picture in Fig. 2(a). As we reported previously,13 copper outdiffusion through a thin and uneven Ta barrier is one possible mechanism for an extrinsic EF. In addition, the reduced confinement effect, due to the uneven and thinner Ta barrier for the preclean-first process, leads to a lower (jLc) product and EM lifetime. The via profiles, shown in Fig. 2, help explain other differences between the two processes. For the preclean-process, the via opening at the top is larger than that of at the via bottom, while a uniform and vertical via is found for barrier-first process. The uneven via profile may not affect EM reliability directly, however, it can be unfavorable for the leakage current and CD control. During the argon plasma preclean process, mechanically weak low-k dielectric is exposed to the argon plasma, resulting in large via opening at the top of the via. However, such a plasma etch damage is minimized for the barrier-first process samples because the predeposited Ta barrier prevents the low-k dielectric from plasma exposure.

Vooids from the EM tested samples were viewed under a optical microscope. The results are expressed in terms of the probability of void formation shown in Fig. 3, which was obtained by dividing the number of lines with a void by the total number of lines. For the preclean-first process, voids were found in most of metal lines longer than 75 μm, and the probability of void formation rapidly decreased in lines shorter than 75 μm. However, for the barrier-first process, the probability of void formation was only about one-half of that of the preclean-first process. With increasing barrier thickness, the probability of void formation decreased even further. These results suggest that barrier process and barrier thickness significantly affect the void formation in the metal lines.

The critical current density and line length product, (jLc), derived statistically are summarized in Fig. 4. The (jLc) product for the pre-clean first process is about 2200 A/cm², which corresponds well with our previous result. The (jLc) product was higher with the barrier-first process than that with the preclean-first process. The difference in the (jLc) product can be attributed to the barrier thickness as shown in Fig. 4. The barrier thicknesses of M2 trench sidewall, obtained from TEM for the different barrier processes and barrier thicknesses, are superimposed with the (jLc) product in Fig. 4. It agrees with our previous work,13 where a linear relationship between the (jLc) product and barrier thickness was found. We also demonstrated that the increase in barrier thickness resulted in an increased effective modulus, as calculated—leading to more confinement effect on the Cu/low-k interconnects. The results suggest that the Ta barrier at the trench sidewall provides the necessary confinement to the Cu lines even if they are surrounded by weak low-k dielec-
The net drift velocity \( v_d \) is the combination of drift velocity induced by EM stress \( (v_{\text{EM}}) \) and drift velocity induced by back-flow stress \( (v_{\text{BF}}) \), which can be expressed as

\[
(v_d) = (v_{\text{EM}}) + (v_{\text{BF}}) = \mu(Z' e p j - \Omega \Delta \sigma / L),
\]

where \( \mu \) is the effective mobility, \( Z' \) is the effective charge, \( e \) is the electronic charge, \( p \) is the electrical resistivity, \( j \) is the current density for EM, \( \Omega \) is the atomic volume, and \( \Delta \sigma / L \) is the EM-induced back-flow stress gradient along the metal line. With increasing barrier thickness, the back-flow stress gradient increases for a given length \( L \), due to the high elastic modulus of the Ta barrier. This leads to a high drift velocity associated with the back-flow stress \( (v_{\text{BF}}) \), and reduces the net drift velocity \( (v_d) \). It is widely known that the dominant diffusion path for Cu interconnects is the interface between copper and the capping layer. In this case, the EM lifetime can be simplified as

\[
\tau = \Delta L_{\text{cr}} / v_d,
\]

where \( \tau \) is the intrinsic EM lifetime induced by surface diffusion, \( \Delta L_{\text{cr}} \) is the critical void length for line failure, and \( v_d \) is the net drift velocity. Since we used a identical test structure for different barrier process splits, \( \Delta L_{\text{cr}} \) was identical. Therefore, The EM lifetime is inversely proportional to the EM drift velocity. From Eqs. (1) and (2), we can deduce that the EM lifetime is proportional to the \((jL)_{\text{c}}\) product. This relationship is borne out in the CDF plots for different barrier processes, as shown in Fig. 5. Therefore, a shorter EM lifetime for the samples with the preclean-first process, as compared with the barrier-first process, can be primarily attributed to the smaller \((jL)_{\text{c}}\) product.

**IV. CONCLUSIONS**

The barrier process effect on the EM reliability of Cu/low-k interconnects has been investigated. Compared with a conventional preclean-first process, extrinsic EF was not observed for the samples with the barrier-first process. This result suggests that the process-induced defects, which are the most probable cause for the early failures, are significantly reduced by the barrier-first process. In addition, TEM micrographs revealed that a more uniform and thicker barrier layer was found at the via and trench for the barrier-first process, than for the preclean first process. A predeposited Ta barrier protected the mechanically weak low-k dielectrics, leading to a uniform via profile; while via erosion was found for preclean-first process due to the argon plasma damage of the dielectric. Critical current density and line length \((jL)_{\text{c}}\) product showed a good correlation with the barrier thickness at the trench sidewall. TEM micrographs revealed that the barrier thickness at the M2 trench sidewall for the barrier-first process was thicker than that of preclean-first process leading to a higher \((jL)_{\text{c}}\) product. This high \((jL)_{\text{c}}\) product effectively increased the drift velocity induced by back-flow stress \( (v_{\text{BF}}) \), thus reducing the net EM drift velocity \( (v_d) \). The reduced net drift velocity prolonged the EM lifetime since the EM lifetime is inversely proportional to the net drift velocity, assuming the interface between copper and the capping layer was the dominant diffusion path for Cu/low-k interconnects fabricated by the damascene process.

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